

Ahsanullah University of Science and Technology Department of Electrical and Electronic Engineering

LABORATORY MANUAL FOR ELECTRICAL AND ELECTRONIC SESSIONAL COURSE

Student Name : Student ID :

> Course no : EEE 2210 Course Title : Electronics Simulation Lab

For the students of Department of Electrical and Electronic Engineering 2nd Year, 2nd Semester Experiment No: 1

Experiment name: Introduction of semiconductor device in Pspice

SEMICONDUCTOR DEVICES

Electronic devices are investigated by examining the device input and output current & voltage characteristics. Device parameters, such as the input and output resistances, current and voltage gains etc, are measured from the characteristics plotted. PSpice allows nested sweep operations where more than one parameter is required to be swept at any given time. For example, plotting the output transistor characteristic requires sweeping the output voltage for a range of swept input base currents.

THE FORWARD AND REVERSE-BIASED DIODE CHARACTERISTIC

Fig.1.1 shows a low-power diode (John Bardeen 1908-1991) in series with a current limiting resistor R1 . The diode current, junction voltage V $_d$, and temperature T (degrees Kelvin) are related:

$$I_d = I_0(e^{q V_d / kT} - 1)$$

Select DC Sweep and enter the parameters shown in Fig. 1.2. We may plot diode current versus the voltage across the cathode & anode by placing a cur marker as shown and sweeping rent the input voltage.



Fig 1.1







Fig 1.3

Diode Temperature Effect:

Use Fig 1.1 for Temperature Effect.



FIGURE Illustrating the temperature dependence of the diode forward characteristic. At a constant current, the voltage drop decreases by approximately 2 mV for every 1°C increase in temperature.

mulation Settings - 12	X
General Analysis Include Fil Analysis type: DC Sweep Options: Primary Sweep Secondary Sweep Monte Carlo/Worst Case Parametric Sweep Save Bias Point Load Bias Point	es Libraries Stimulus Options Data Collection Probe Window C Run the simulation at temperature: C Repeat the simulation for each of the temperatures: 50 100 150 C Enter a list of temperatures, separated by spaces. For example, 0 27 125
	OK Cancel Apply Help

Temperature: 50.0, 100.0, 150.0



Describing the Diode Characteristic of Tabular Data:

Use the PSpice to calculate the operating point (V_D, I_D) . The diode characteristic is represented by the following table:

I _D	0	10	20	30	40	50	60	70
V _D	0.5	0.87	0.98	1.058	1.115	1.173	1.212	1.125

For operating point we have to use .OP command. And also Piecewise-linear model of the diode characteristic and its equivalent is used.





TABLE = (0,0) (1n,0.5) (10m,0.87) (20m,0.98) (30m,1.058) (40m,1.115) (50m,1.173) (60m,1.212) (70m,1.250)

**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 15.0000 (2) 15.0000 (3) 13.9580

VOLTAGE SOURCE CURRENTS

NAME CURRENT

- V_Vx 2.792E-02
- V_V1 -2.792E-02

TOTAL POWER DISSIPATION 4.19E-01 WATTS

**** 11/19/10 14:41:38 ******* PSpice 9.2 (Mar 2000) ******* ID# 0 *******

** Profile: "SCHEMATIC1-11" [J:\EEE2210(solved)\Lab 01\etable-SCHEMATIC1-11.sim]

**** VOLTAGE-CONTROLLED VOLTAGE SOURCES

 NAME
 E_E1

 V-SOURCE
 1.042E+00

 I-SOURCE
 2.792E-02

JOB CONCLUDED

TOTAL JOB TIME .03

FULL WAVE BRIDGE RECTIFIER:







Using Transformer:

To use transformer we will use XFRM_LINEAR. Normal where the parameters are L1=100uH, L2=10uH and Coupling=1



FULL WAVE BRIDGE RECTIFIER WITH R-C FILTER:

It is possible to further reduce the amount of ripple across a filter capacitor by using an additional RC filter section as shown in Fig. 19.8. The purpose of the added RC section is to pass most of the dc component while attenuating (reducing) as much of the ac component as possible.

Figure shows a full-wave rectifier with capacitor filter followed by an RC filter section. The operation of the filter circuit can be analyzed using superposition for the dc and ac components of signal.



Report:

1. A full-wave diode circuit with a center-tapped step down transformer of turn ratios 6:1 is supplying a load $R_L = 1$ KW as shown. A 10 m F capacitor is added to smooth the ripple. R_2 is added to provide a voltage divider so as to control the voltage across R_L . The diode model is 1N4002. The supply voltage amplitude is 169 V, and its frequency is 60Hz. Use transient analysis to plot the voltage across R_L .



2. Is it possible to improve the above circuit? If yes, then improve the above circuit.

Experiment No: 2

Experiment name: Diode Analysis

Clipper and Clamper Circuit:

Design a clipper circuit to clip off the portion of an input voltage that falls above 9 V or below -5 V. Use 1N4002 diodes which has a voltage drop of approximately 0.7 V. V1 = 9 - 0.7 = 8.3 V, V2 = 5 - 0.7 = 4.3 V. The input is a sine wave of 16 V amplitude and 60 Hz frequency. R1 = 1K to limit the forward diode current. Use transient analysis with a final time of 33.33 ms and a step ceiling of 0.01ms. Plot the input and output voltage waveform. On a separate graph obtain plot the transfer characteristic Vo versus Vin.



Fig 2.1



Zener Diode:

Obtain the I-v characteristic of the Zener diode (D1N750 is a 4.7 V Zener). The voltage regulator circuit shown below has R = 1 KW and uses Zener diode D1N750.

- What is the output voltage when the supply voltage is dropped to V1 = 8 V?
- Find the output voltage for V1 = 16 V.
- Find *i-v* curve.



Construct the above schematic and label the output node as V_{out} . Select the setup from the analysis menu, click the DC Sweep dialog button. The DC sweep dialog box appears. For the Sweep variable type select the voltage source, and set its name to V1. Using the sweep type linear, set the starting value to 0, end value to 20 and increment to 0.05.

When simulation is complete probe graphic window appears. From the Plot pull-down menu select X Axis Settings, click the Axis Variable button to open the variable list, and select V(Vout) to be the horizontal axis. Click OK button and the Zener diode i-v characteristic is displayed as shown.

Now we can draw the load lines corresponding to V1 = 16 V, and V1 = 8 V. From KVL we have $V_i=R_i+V_{out.}$

(a) When i = 0, Vout = V1 = 16 V and when Vout= 0, i = 16/1000 = 16 mA

In Probe from Tools pull-down menu select Label/Line and draw the above line. Enable the Cursor and move the operating point and from the Tools

select Label/Mark to mark the coordinates of the operating point. The output voltage is found to be 4.6698 V.

(b) Repeat (a) for V1 = 6 V. The output voltage is found to be 4.5964 V. This represent a drop in the output voltage of less than 1.57 percent when the

input voltage is changed form 16 V to 8 V.



Application of Zener Diode:

A Zener diode (1N750) is added to the circuit to have a 4.7 V regulated DC power supply. Use transient analysis to plot the voltage $acrossR_L$. The Zener diode 1N750 has a breakdown voltage of 4.7 V.



Square Wave Generator:

Fig. 2.4 is a voltage piece-wise linear (VPWL) part where the input signal source, after selection and Rclicking/Edit Properties, has the time–voltage pair values entered in the spreadsheet Fig. 2.5 shows how the zener diode limits the amplitude of the output signal. To plot the output voltage for a range of input voltage–the transfer function) shown in Fig. 2.6, we need to change the x-axis from Time to the input voltage v1(Vin). We do this from Probe by selecting an x-axis number and from the menu select Axis Variable. Highlighting V1(Vin) from the list automatically places it in the Trace Expression box, so press OK.



Fig 2.5



Report:

Use Zener Diode to improve the voltage regulator circuit.

EXP:03 Concept of BJT, JFET, MOSFET in Pspice

Objective: In this lab we will cover the circuits taught in Electronics-I and Electronics –II. Orcad PSPCE 9.2 is used as a simulation tools. Students are suggested to review EEE-1210 lab sheets to brush up the basic of PSPICE.

Reference Book:

SPICE FOR CIRCUITS AND ELECTRONICS USING PSPICE. By Dr. Harun-Ur-Rashid

COMMON BASE BJT CHARACTERISTIC:

What follows is a computer analysis comparing a PSpice nonlinear model of the 2N3904 (NPN) BJT with a piecewise linear (Ebers-Moll) model of the same device. Concurrently the qualitative description of device phenomena is used to compare the 'experimental' computer data with what would be expected. The transistor is connected in a 'common base' configuration, meaning simply that the base provides the common terminal between the input and output ports. To illustrate the basic device performance the 'collector' characteristics are computed. These are a set of parametric curves showing collector current vs. collector voltage, with a fixed emitter current for each curve. The netlist on the right, below, provides the PSpice input corresponding to the circuit drawn on the left. The collector-base voltage is swept for several parametric values of the emitter current.

We start examination of the plot with the characteristic for IE = 0; since the emitter junction is OFF this is essentially the collector junction diode characteristic. Since essentially no electrons are injected into the base there is no transport across the base and no augmentation of the collector junction current. (Because the collector junction normally operates in reverse-bias the polarity conventions used for the transistor are such as to make collector junction forward-bias current negative; the exponential part of the junction characteristic thus appears on the left side of the transistor plot. This puts what will be the more interesting part of the characteristics in the first quadrant.)

Now note that the other characteristics essentially are displacements of the IE = 0 characteristic, i.e., the injected current (actually a slightly smaller amount) simply adds to the intrinsic collector junction current. The current displacement increment is slightly smaller than the emitter current increment because there is a small loss of injected carriers to hole recombination as they cross the base. However generally the loss is unlikely to be as large as 5% and more than likely will be closer to 1% of the carrier flow.

In the 'normal' operating mode (emitter junction forward-biased, collector junction reverse-biased) the characterization of the transistor as a controlled current source is clearly appropriate. Actually the

collector junction can be s l ightly forward -biased before current is injected by the c ollector back into the base; a junction has very small forward current for a forward bias below a 'knee' voltage of roughly 0.5 volt (for silicon).



** Profile: "SCHEMATIC1-minhaz" [C:\EXAMPLE\pspice\z... Date/Time run: 09/10/08 19:54:41



COMMON EMITTER BJT CHARACTERISTICS:



Primary DC SWEEP: V2 i.e. voltage source VCE from 1V to 3V with the increment of 0.1V

Secondary DC sweep : I1 i.e. base current from 0uA to 20uA with the increment of 5uA.







Objective: In this lab we will cover the circuits related to OP-AMP. Students should go through the theory and application of Opamp.

Reference Book:

- 1. SPICE FOR CIRCUITS AND ELECTRONICS USING PSPICE. By Dr. Harun-Ur-Rashid
- 2. Operational Amplifiers and Linear Integrated Circuits. By-Robert F.Coughlin & Frederick F.Driscoll



Non-Inverting Amplifier:



Inverting Amplifier:





Buffer:



Adder:



Page 1



: November 05, 2008



Time: 15:57:04



Experiment No: 5

Experiment name: Application of Opamp

Slew Rate, SR

Another parameter reflecting the op-amp's ability to handling varying signals is slew rate, defined as

$$SR = \frac{\Delta V_0}{\Delta t} \quad V/\mu s \quad \text{with t in } \mu s \text{ sec}$$

The slew rate provides a parameter specifying the maximum rate of change of the output voltage when driven by a large step-input signal. If one tried to drive the output at a rate of voltage change greater than the slew rate, the output would not be able to change fast enough and would not vary over the full range expected, resulting in signal clipping or distortion. In any case, the output would not be an amplified duplicate of the input signal if the op-amp slew rate is exceeded.



Fig 6.1: Inverting mode opamp



The VSIN part has Freq set to 100 kHz, VAMP = 1 V (A peak value), and VOFF = 0. [Note there is no space between the variable value and the dimensions, i.e. 100k, not 100 k as this will produce an error "ERROR – Expecting keyword STIMULUS, saw k"]. Carry out a transient analysis with Run to time = 50 us, Maximum step size = 100 n and compare the slewed output signal in Fig. 6.2 to the input sine wave. Simulating a schematic produces several files, one of which is the Probe output called.dat file which when selected from Probe should produce a blank screen, so click *Trace/Add* Trace, and select the output signal (Or press the Insert key). To measure the output distortion for different input voltages, open the *Analysis Setup/Transient* menu Click on *Output File Option*. Place a tick on Perform *Fourier Analysis*, Center frequency = 100 k, Number of Harmonics = 10, and Output Variables: = v(vout). From Probe, select the icon from the left-hand toolbar to examine the harmonic analysis information at the end of the .out text file.

** Profile: "SCHEMATIC1-41" [J:\EEE2210(solved)\Lab 01\sr rate-SCHEMATIC1-41.sim]

**** FOURIER ANALYSIS TEMPERATURE = 27.000 DEG C FOURIER COMPONENTS OF TRANSIENT RESPONSE V(OUT) DC COMPONENT = -2.973421E-01 HARMONIC FREQUENCY FOURIER NORMALIZED NORMALIZED PHASE PHASE (DEG) NO (HZ) COMPONENT COMPONENT (DEG) 1 1.000E+05 1.003E+001.000E+00 9.471E+01 0.000E+00 2 2.000E+05 1.300E-03 1.297E-03 4.066E+01 -1.488E+02 3 3.000E+05 1.078E-01 1.075E-01 1.051E+02 -1.790E+02 4 4.000E+05 7.613E-04 1.055E+02 -2.733E+02 7.635E-04 5 5.000E+05 3.663E-02 3.653E-02 1.159E+02 -3.577E+02 6.000E+05 9.129E-04 9.104E-04 1.392E+02 -4.290E+02 6 7 7.000E+05 1.730E-02 1.725E-02 1.275E+02 -5.354E+02

8	8.000E+05	1.088E-03	1.085E-03	1.569E+02	-6.007E+02
9	9.000E+05	9.630E-03	9.604E-03	1.403E+02	-7.121E+02
10	1.000E+06	1.227E-03	1.224E-03	1.690E+02	-7.780E+02

TOTAL HARMONIC DISTORTION = 1.153108E+01 PERCENT

Gain-Bandwidth Product:



A *PARAM* part investigates the concept of *GAIN–BANDWIDTH* product and shows how the gain and bandwidth parameters are interlinked i.e. if the gain is reduced then the bandwidth increased and vice versa.

Rclick the *PARAM* part, select Edit Properties and add a new row with **Ra** entered in the first column and **1k** in the second column. Go back to the schematic and select the resistance Ra and enter {Ra} rather than an actual resistance value. We wish to carry out a frequency response for the different values of the resistor to be swept, so select the *Analysis tab* from the simulation icon and select Analysis type: *AC Sweep/Noise*, *AC Sweep Type to Linear*, *Start Frequency* = 10, *End Frequency* = 1000k, *Points/Decade* = 1000. Tick Parametric Sweep in the Options menu and set the parameters shown in Fig. 6.2. Enter the values for *Ra* in the Value List with each value separated by a space.

Press F11, and a Probe screen message "*Available Sections*" appears. Select *OK* to plot the frequency response as shown in Fig. 8.9. Measure the passband gain and -3 dB point on each response.

The gain-bandwidth product is investigated using *Performance Analysis (PA)* available in *Probe/Trace menu*. PA allows you see how a characteristic, such as the gain bandwidth



Fig 6.3: Noninverting frequency response



Fig6.4 :GB product using Performance Analysis

product in this case, varies when the feedback resistor, **Ra** is varied. Simulate the previous schematic, and from the Probe output, press ok from Available Sections. Press the PA icon (Two crossed flags) and a further menu headed Performance Analysis appears, so press OK. Select the **Trace Add icon** and enter *Cutoff Lowpass 3dB(V(vout))*Max(V(vout))* in the Trace Expression box to produce the display in Fig. 6.4

Free Running Multivibrator:



Fig 6.5: Free Running Multivibrator



A free running multivibrator is a square generator. Here the equation for upper threshold voltage and Lower threshold voltage is

$$V_{ut} = \frac{R_2}{R_1 + R_2} (+ V_{sat})$$

$$V_{lt} = \frac{R_2}{R_1 + R_2} \left(-V_{sat}\right)$$

Here R_1 =100k and R_2 =86k.

Exp: 6 ACTIVE FILTER

Objective: In this lab we will cover the circuits related with Active filter. We have covered Low, High, Band pass & Band-rejection filter in AC circuit which was designed using passive elements. But in this lab, we will design and simulate those filters using OPAMP. Using OPAMP creates reliability, high gain and sharper cut -off of the desired signal.

Reference Book: ACTIVE FILTER, Chapter-11, By: Coughlin

Due to limitations of the op-amp, frequencies above 1MHz are unachievable.

LOW PASS FILTER:



-40db/decade:

-60db/decade:







HIGH PASS FILTER:



-40db/decade:

-60db/decade:



OUTPUT of these three High pass filters in db:



BANDPASS FILTER/Basic wideband filter:



Objective: In this lab we will cover the circuits related to Oscillator.

Reference Book:

1. SPICE FOR CIRCUITS AND ELECTRONICS USING PSPICE. By Dr. Harun-Ur-Rashid

2. Operational Amplifiers and Linear Integrated Circuits. By-Robert F.Coughlin & Frederick F.Driscoll

OSCILLATOR:

Relaxation Oscillator (Free Running multivibrator):





Phase Shift Oscillator using BJT:





